Research and Development Lixia Tang

ECN#

360.2

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## \_twirlight

## **ENGINEERING CHANGE NOTE:**



360.2

ECN#:

ASSEMBLY:	BMW4041D	DESCRIPTION:	MW4-QDC Quad Digital Channel Card
New Assembly:		DATE:	17/10/00
<b>Current Assy Rev:</b>	F	<b>Current Schematic Rev:</b>	
New Assy Rev:	G 1G	New Schematic Rev:	
CMS BOMs Update	ed • Excel BOMs Updated	O Subcontractor Records Up	odated Compatibility Maintained: Yes
IMPLEMENTATION INFORMATION:			
O Safety Issue	UL Compliance Issue	O New Feature	Cost Reduction
• Bug Fix	EMC Compliance Issue		0.000 0.000 0.000
Reliability Reason	^	Cosmetic Change	
REASON FOR CHANGE:  Correct mistakes in the BOM Improve DSP and ADV clock signals			
DETAILS OF CHANGE:			
1. Fit a 1k5 SMD 0603 resistor Fairlight P/N RMD7490 at each of the following locations: R5, R15, R307, R310, R314, R316 on QDC rev4 boards.			
2. Fit a 220r SMD 0603 resistor Fairlight P/N RMD4319 at location R313			
3. On solder side, cut track from U145/4 to R307 (This is a very short track). Reconnect same pad of R307 to U145/3			
4. Inspect ICs U112-U115 and U123-U126 (8 x CY7C024 DPRAMS)			
If any of these 8 parts have a speed grade = 25 ns then add a solder blob across J5 and place a assembly revision label after the blank PCB P/N on the card, marked "1G", so it looks as follow: "BMW4041D-1G"			
If all 8 parts are speed grade 15 or 20 ns then there should be no solder blob on J5 and place a assembly revision label after the blank PCB P/N on the card, marked "G", so it looks as follow: "BMW4041D-G"			

ECN360.2 is a correction to ECN 360.1: Changed "G" to "G 1G" in NEW ASSY REV